2.5-W MONO FILTER-FREE CLASS-D AUDIO POWER AMPLIFIER

FEATURES

- **Maximum Battery Life and Minimum Heat**
  - **Efficiency With an 8-Ω Speaker:**
    - **88% at 400 mW**
    - **80% at 100 mW**
  - **2.8-mA Quiescent Current**
  - **0.5-µA Shutdown Current**
- **Only Three External Components**
  - **Optimized PWM Output Stage Eliminates LC Output Filter**
  - **Internally Generated 250-kHz Switching Frequency Eliminates Capacitor and Resistor**
  - **Improved PSRR (–75 dB) and Wide Supply Voltage (2.5 V to 5.5 V) Eliminates Need for a Voltage Regulator**
  - **Fully Differential Design Reduces RF Rectification and Eliminates Bypass Capacitor**
  - **Improved CMRR Eliminates Two Input Coupling Capacitors**
- **Wafer Chip Scale Packaging (WCSP)**
  - **NanoFree™ Lead-Free (YZF)**
  - **NanoStar™ SnPb (YEF)**

APPLICATIONS

- **Ideal for Wireless or Cellular Handsets and PDAs**

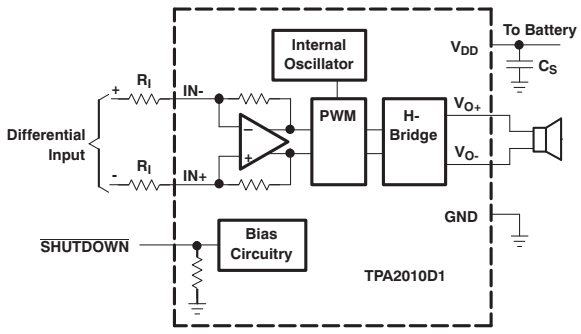
DESCRIPTION

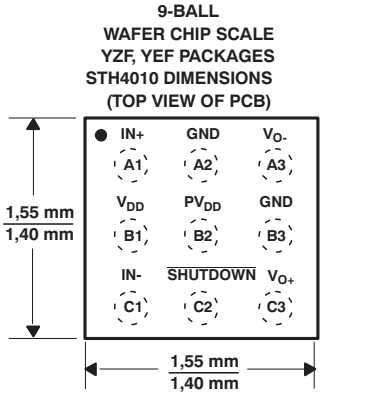
The STH4010 is a 2.5-W high efficiency filter-free class-D audio power amplifier (class-D amp) in a 1,45 mm × 1,45 mm wafer chip scale package (WCSP) that requires only three external components.

Features like 88% efficiency, –75-dB PSRR, improved RF-rectification immunity, and 8 mm^2 total PCB area make the STH4010 class-D amp ideal for cellular handsets. A fast start-up time of 1 ms with minimal pop makes the STH4010 ideal for PDA applications.

In cellular handsets, the earpiece, speaker phone, and melody ringer can each be driven by the STH4010. The STH4010 allows independent gain while summing signals from seperate sources, and has a low 36 µV noise floor, A-weighted.

APPLICATION CIRCUIT





Note: Pin A1 is marked with a "0" for Pb-free (YZF) and a "1" for SnPb (YEF).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGE	PART NUMBER	SYMBOL
–40°C to 85°C	Wafer chip scale package (YEF)	STH4010YEF (1)	AJZ
	Wafer chip scale packaging – Lead free (YZF)	STH4010YZF (1)	AKO

(1) The YEF and YZF packages are only available taped and reeled. To order add the suffix *R* to the end of the part number for a reel of 3000, or add the suffix *T* to the end of the part number for a reel of 250 (e.g. STH4010YEFR).

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			STH4010
V_{DD}	Supply voltage	In active mode	–0.3 V to 6 V
		In $\overline{\text{SHUTDOWN}}$ mode	–0.3 V to 7 V
V_I	Input voltage		–0.3 V to V_{DD} + 0.3 V
	Continuous total power dissipation		See Dissipation Rating Table
T_A	Operating free-air temperature		–40°C to 85°C
T_J	Operating junction temperature		–40°C to 125°C
T_{stg}	Storage temperature		–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	YZF	260°C
		YEF	235°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		2.5		5.5	V
V_{IH}	High-level input voltage	$\overline{\text{SHUTDOWN}}$	1.3		V_{DD}	V
V_{IL}	Low-level input voltage	$\overline{\text{SHUTDOWN}}$	0		0.35	V
R_I	Input resistor	Gain ≤ 20 V/V (26 dB)	15			kΩ
V_{IC}	Common mode input voltage range	V_{DD} = 2.5 V, 5.5 V, CMRR ≤ –49 dB	0.5		V_{DD}–0.8	V
T_A	Operating free-air temperature		–40		85	°C

PACKAGE DISSIPATION RATINGS

PACKAGE	DERATING FACTOR(1)	$T_A \le 25°C$ POWER RATING	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
YEF	7.8 mW/°C	780 mW	429 mW	312 mW
YZF	7.8 mW/°C	780 mW	429 mW	312 mW

(1) Derating factor measure with High K board.

ELECTRICAL CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OS}\|$	Output offset voltage (measured differentially)	V_I = 0 V, A_V = 2 V/V, V_{DD} = 2.5 V to 5.5 V		1	25	mV
PSRR	Power supply rejection ratio	V_{DD} = 2.5 V to 5.5 V		–75	–55	dB
CMRR	Common mode rejection ratio	V_{DD} = 2.5 V to 5.5 V, V_{IC} = V_{DD}/2 to 0.5 V, V_{IC} = V_{DD}/2 to V_{DD} –0.8 V		–68	–49	dB
$\|I_{IH}\|$	High-level input current	V_{DD} = 5.5 V, V_I = 5.8 V			100	µA
$\|I_{IL}\|$	Low-level input current	V_{DD} = 5.5 V, V_I = –0.3 V			5	µA
$I_{(Q)}$	Quiescent current	V_{DD} = 5.5 V, no load		3.4	4.9	mA
		V_{DD} = 3.6 V, no load		2.8		
		V_{DD} = 2.5 V, no load		2.2	3.2	
$I_{(SD)}$	Shutdown current	$V_{\overline{(SHUTDOWN)}}$= 0.35 V, V_{DD} = 2.5 V to 5.5 V		0.5	2	µA
$r_{DS(on)}$	Static drain-source on-state resistance	V_{DD} = 2.5 V		700		mΩ
		V_{DD} = 3.6 V		500		
		V_{DD} = 5.5 V		400		
	Output impedance in $\overline{SHUTDOWN}$	$V_{\overline{(SHUTDOWN)}}$ = 0.4 V		>1		kΩ
$f_{(sw)}$	Switching frequency	V_{DD} = 2.5 V to 5.5 V	200	250	300	kHz
	Gain	V_{DD} = 2.5 V to 5.5 V	$\frac{285\ k\Omega}{R_I}$	$\frac{300\ k\Omega}{R_I}$	$\frac{315\ k\Omega}{R_I}$	$\frac{V}{V}$
	Resistance from shutdown to GND			300		kΩ

OPERATING CHARACTERISTICS

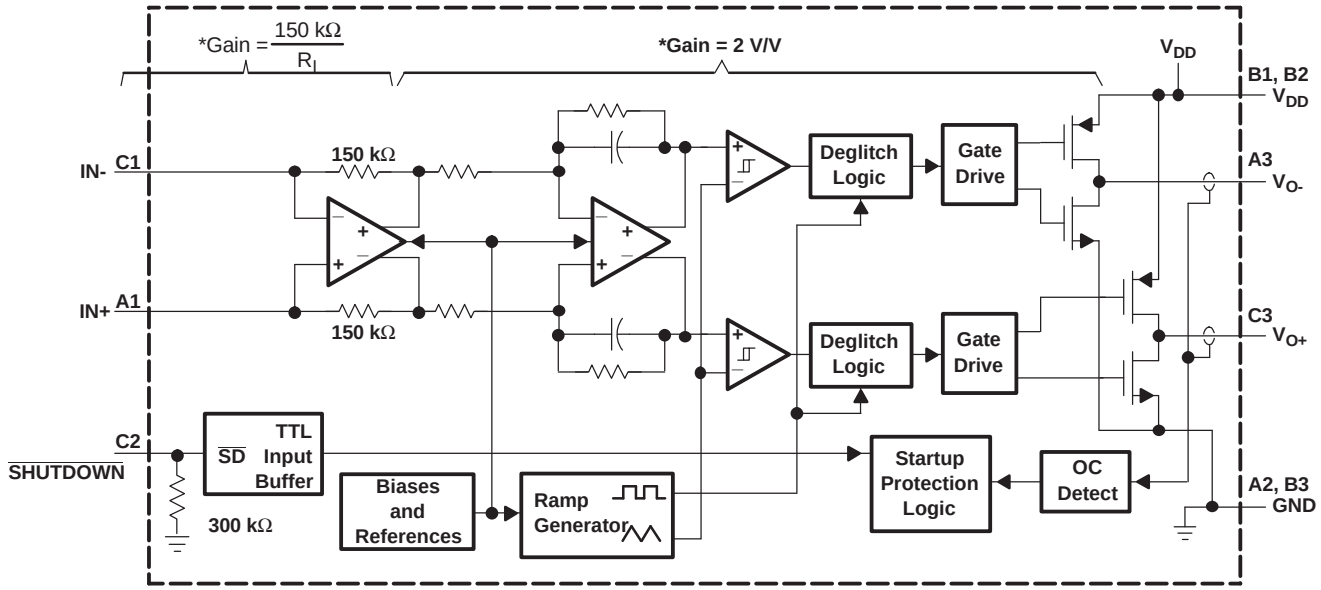
T_A = 25°C, Gain = 2 V/V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD + N = 10%, f = 1 kHz, R_L = 4 Ω	V_{DD} = 5 V		2.5		W
			V_{DD} = 3.6 V		1.3		
			V_{DD} = 2.5 V		0.52		
		THD + N = 1%, f = 1 kHz, R_L = 4 Ω	V_{DD} = 5 V		2.08		W
			V_{DD} = 3.6 V		1.06		
			V_{DD} = 2.5 V		0.42		
		THD + N = 10%, f = 1 kHz, R_L = 8 Ω	V_{DD} = 5 V		1.45		W
			V_{DD} = 3.6 V		0.73		
			V_{DD} = 2.5 V		0.33		
		THD + N = 1%, f = 1 kHz, R_L = 8 Ω	V_{DD} = 5 V		1.19		W
			V_{DD} = 3.6 V		0.59		
			V_{DD} = 2.5 V		0.26		
THD+N	Total harmonic distortion plus noise	V_{DD} = 5 V, P_O = 1 W, R_L = 8 Ω, f = 1 kHz			0.18%		
		V_{DD} = 3.6 V, P_O = 0.5 W, R_L = 8 Ω, f = 1 kHz			0.19%		
		V_{DD} = 2.5 V, P_O = 200 mW, R_L = 8 Ω, f = 1 kHz			0.20%		
k_{SVR}	Supply ripple rejection ratio	V_{DD} = 3.6 V, Inputs ac-grounded with C_i = 2 µF	f = 217 Hz, $V_{(RIPPLE)}$ = 200 mV_{pp}		–67		dB
SNR	Signal-to-noise ratio	V_{DD} = 5 V, P_O = 1 W, R_L = 8 Ω			97		dB
V_n	Output voltage noise	V_{DD} = 3.6 V, f = 20 Hz to 20 kHz, Inputs ac-grounded with C_i = 2 µF	No weighting		48		μV_{RMS}
			A weighting		36		
CMRR	Common mode rejection ratio	V_{DD} = 3.6 V, V_{IC} = 1 V_{pp}	f = 217 Hz		–63		dB
Z_I	Input impedance			142	150	158	kΩ
	Start-up time from shutdown	V_{DD} = 3.6 V			1		ms

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	YEF, YZF		
IN–	C1	I	Negative differential input
IN+	A1	I	Positive differential input
V_{DD}	B1	I	Power supply
V_{O+}	C3	O	Positive BTL output
GND	A2, B3	I	High-current ground
V_{O-}	A3	O	Negative BTL output
$\overline{SHUTDOWN}$	C2	I	Shutdown terminal (active low logic)
PVDD	B2	I	Power supply

FUNCTIONAL BLOCK DIAGRAM



Notes:

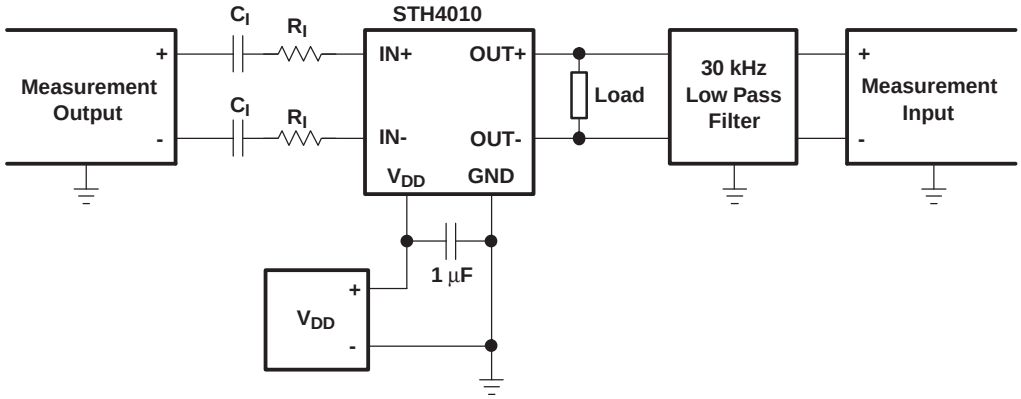
* Total gain = $2 \times \frac{150\ k\Omega}{R_I}$

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

			FIGURE
	Efficiency	vs Output power	1, 2
P_D	Power dissipation	vs Output power	3, 4
	Supply current	vs Output power	5, 6
$I_{(Q)}$	Quiescent current	vs Supply voltage	7
$I_{(SD)}$	Shutdown current	vs Shutdown voltage	8
P_O	Output power	vs Supply voltage	9
		vs Load resistance	10, 11
THD+N	Total harmonic distortion plus noise	vs Output power	12, 13
		vs Frequency	14, 15, 16, 17
		vs Common-mode input voltage	18
K_{SVR}	Supply voltage rejection ratio	vs Frequency	19, 20, 21
	GSM power supply rejection	vs Time	22
		vs Frequency	23
K_{SVR}	Supply voltage rejection ratio	vs Common-mode input voltage	24
CMRR	Common-mode rejection ratio	vs Frequency	25
		vs Common-mode input voltage	26

TEST SET-UP FOR GRAPHS



Notes:
(1) C_I was Shorted for any Common-Mode input voltage measurement
(2) A 33-µH inductor was placed in series with the load resistor to emulate a small speaker for efficiency measurements.
(3) The 30-kHz low-pass filter is required even if the analyzer has an internal low-pass filter. An RC low pass filter (100 Ω, 47 nF) is used on each output for the data sheet graphs.

EFFICIENCY vs OUTPUT POWER

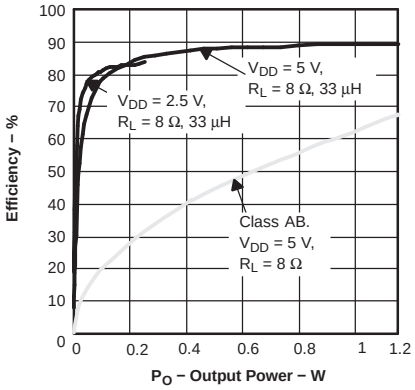


Figure 1.

EFFICIENCY vs OUTPUT POWER

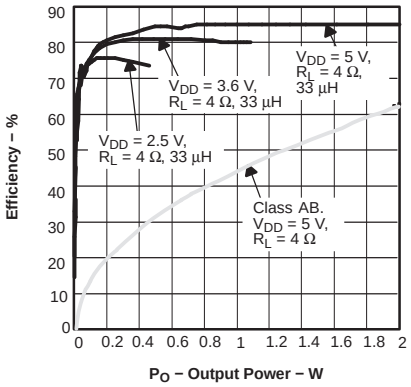


Figure 2.

POWER DISSIPATION vs OUTPUT POWER

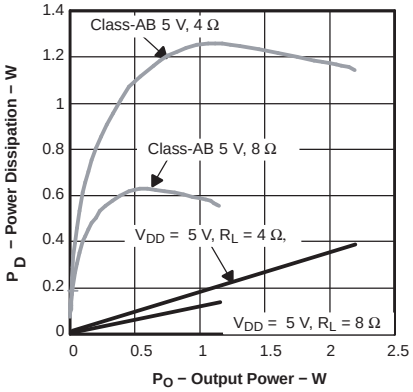


Figure 3.

POWER DISSIPATION vs OUTPUT POWER

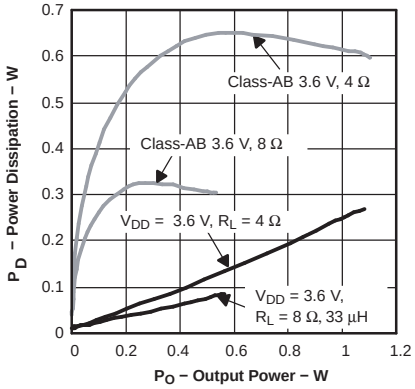


Figure 4.

SUPPLY CURRENT vs OUTPUT POWER

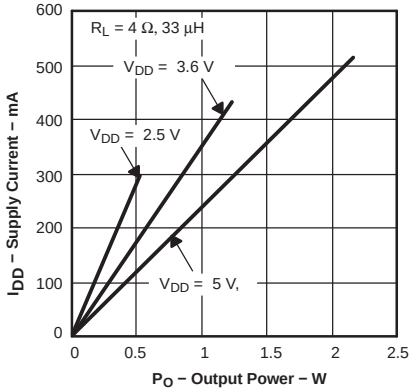


Figure 5.

SUPPLY CURRENT vs OUTPUT POWER

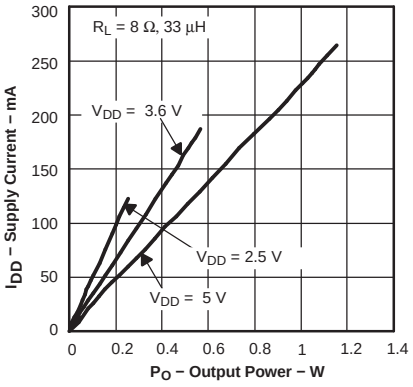


Figure 6.

SUPPLY CURRENT vs SUPPLY VOLTAGE

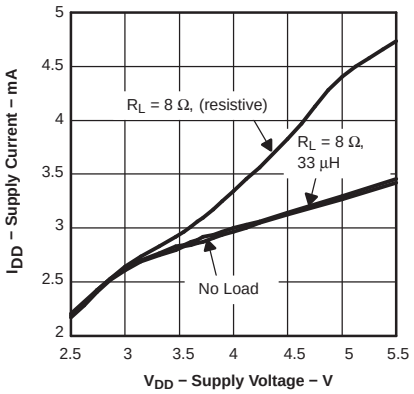


Figure 7.

SUPPLY CURRENT vs SHUTDOWN VOLTAGE

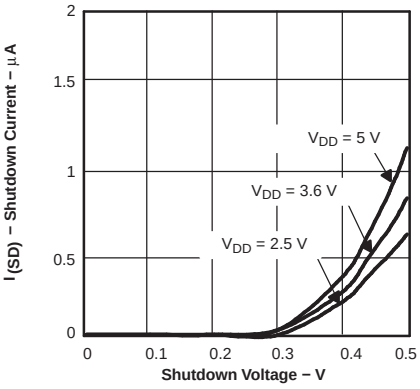


Figure 8.

OUTPUT POWER vs LOAD RESISTANCE

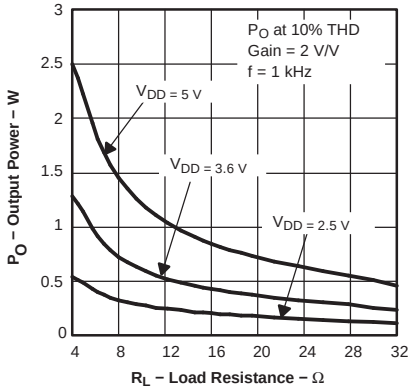


Figure 9.

OUTPUT POWER vs LOAD RESISTANCE

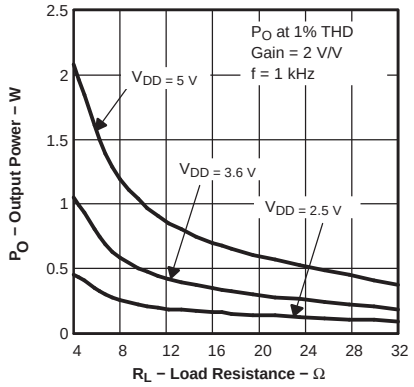


Figure 10.

OUTPUT POWER vs SUPPLY VOLTAGE

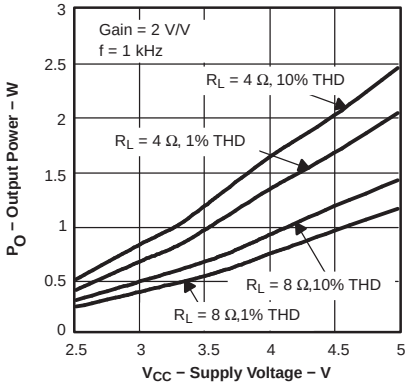


Figure 11.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

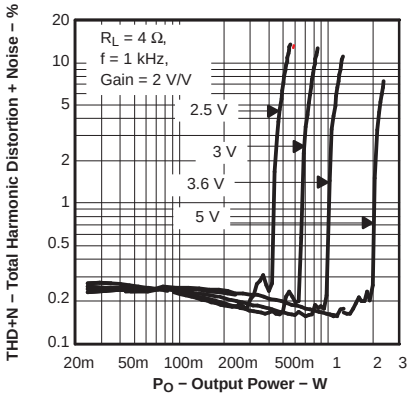


Figure 12.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

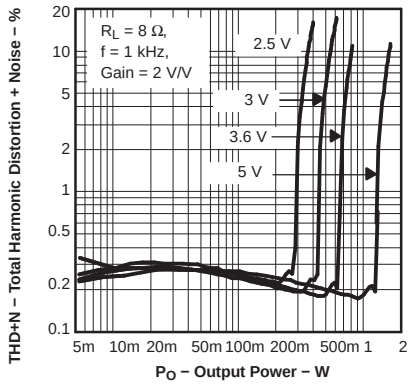


Figure 13.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

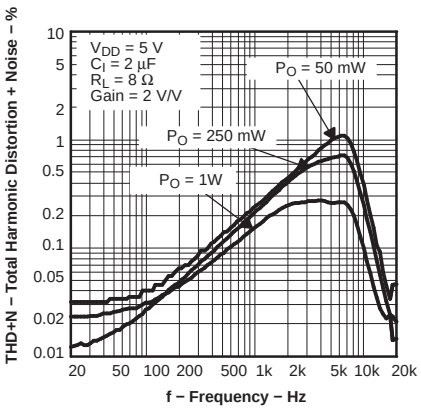


Figure 14.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

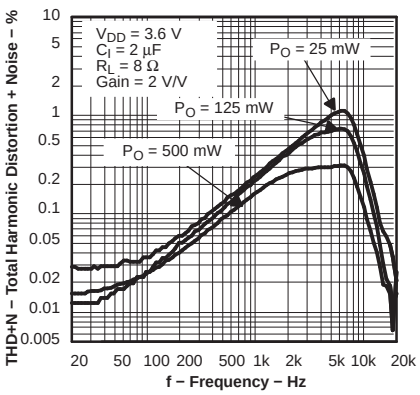


Figure 15.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

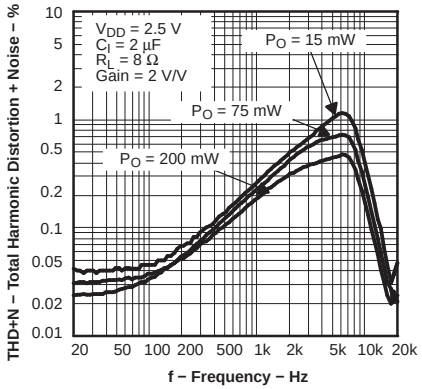


Figure 16.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

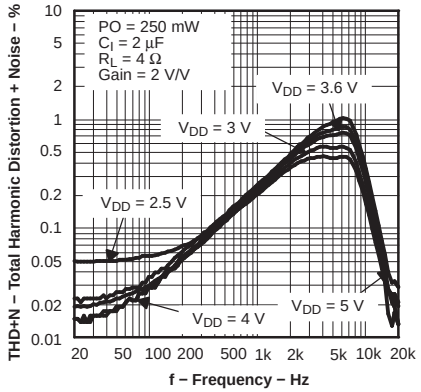


Figure 17.

TOTAL HARMONIC DISTORTION + NOISE vs COMMON MODE INPUT VOLTAGE

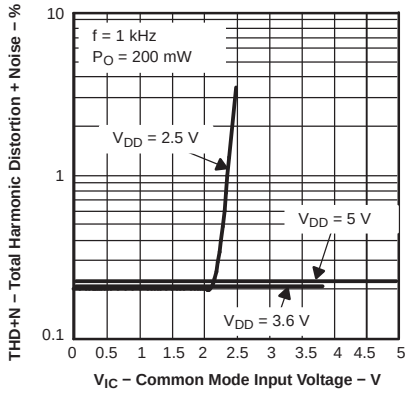


Figure 18.

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

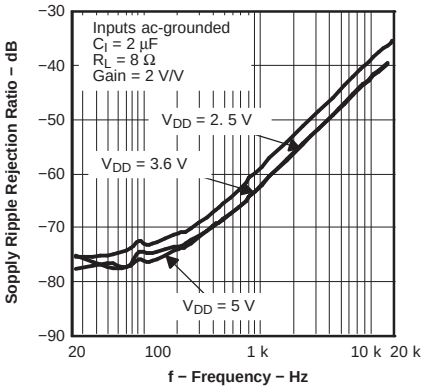


Figure 19.

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

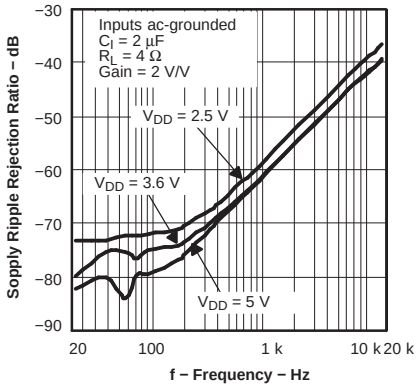
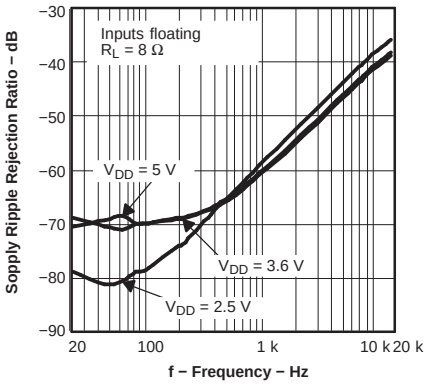


Figure 20.

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY



GSM POWER SUPPLY REJECTION vs TIME

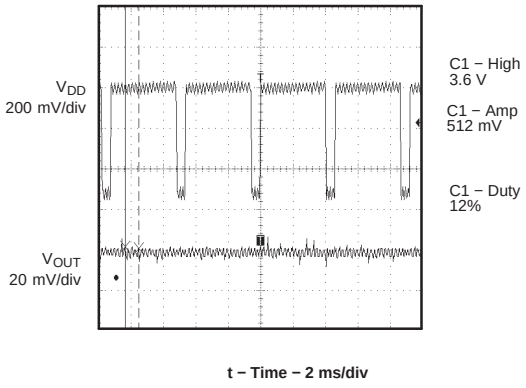


Figure 22.

GSM POWER SUPPLY REJECTION vs FREQUENCY

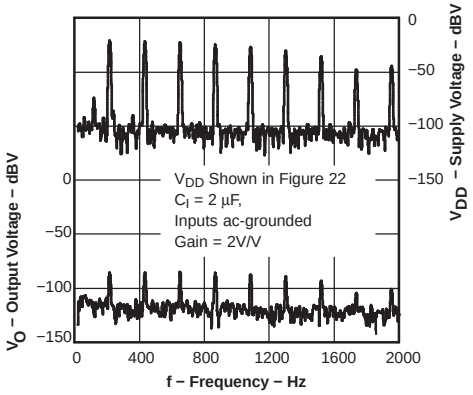


Figure 23.

SUPPLY RIPPLE REJECTION RATIO vs DC COMMON MODE VOLTAGE

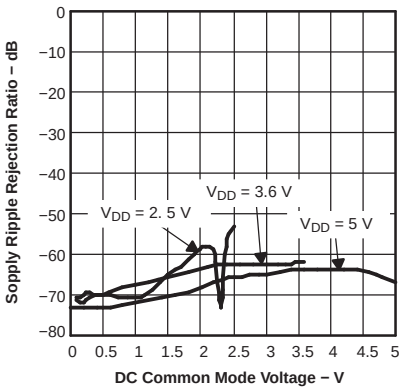


Figure 24.

COMMON-MODE REJECTION RATIO vs FREQUENCY

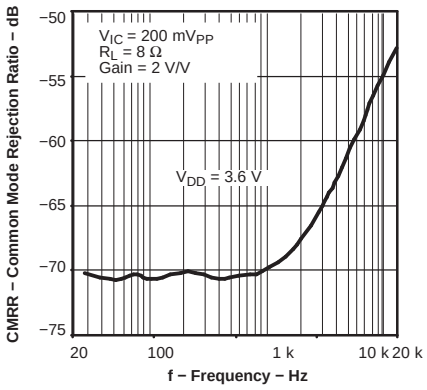


Figure 25.

COMMON-MODE REJECTION RATIO vs COMMON-MODE INPUT VOLTAGE

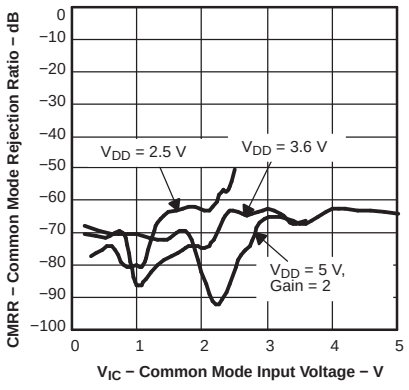


Figure 26.

APPLICATION INFORMATION

FULLY DIFFERENTIAL AMPLIFIER

The STH4010 is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage on the output that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around $V_{DD}/2$ regardless of the common-mode voltage at the input. The fully differential STH4010 can still be used with a single-ended input; however, the STH4010 should be used with differential inputs when in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

Advantages of Fully DIfferential Amplifiers

- Input-coupling capacitors not required:
  - The fully differential amplifier allows the inputs to be biased at voltage other than mid-supply. For example, if a codec has a midsupply lower than the midsupply of the STH4010, the common-mode feedback circuit will adjust, and the STH4010 outputs will still be biased at midsupply of the STH4010. The inputs of the STH4010 can be biased from 0.5 V to V_{DD} – 0.8 V. If the inputs are biased outside of that range, input-coupling capacitors are required.
- Midsupply bypass capacitor, $C_{(BYPASS)}$, not required:
  - The fully differential amplifier does not require a bypass capacitor. This is because any shift in the midsupply affects both positive and negative channels equally and cancels at the differential output.
- Better RF-immunity:
  - GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 217 Hz. The transmitted signal is picked-up on input and output traces. The fully differential amplifier cancels the signal much better than the typical audio amplifier.

COMPONENT SELECTION

Figure 27 shows the STH4010 typical schematic with differential inputs and Figure 28 shows the STH4010 with differential inputs and input capacitors, and Figure 29 shows the STH4010 with single-ended inputs. Differential inputs should be used whenever possible because the single-ended inputs are much more susceptible to noise.

Table 1. Typical Component Values

REF DES	VALUE	EIA SIZE	MANUFACTURER	PART NUMBER
R_I	150 kΩ (±0.5%)	0402	Panasonic	ERJ2RHD154V
C_S	1 µF (+22%, -80%)	0402	Murata	GRP155F50J105Z
C_I (1)	3.3 nF (±10%)	0201	Murata	GRP033B10J332K

(1) C_I is only needed for single-ended input or if V_{ICM} is not between 0.5 V and V_{DD} – 0.8 V. C_I = 3.3 nF (with R_I = 150 kΩ) gives a high-pass corner frequency of 321 Hz.

Input Resistors (R_I)

The input resistors (R_I) set the gain of the amplifier according to Equation 1.

$$\text{Gain} = \frac{2 \times 150\ \text{k}\Omega}{R_I} \quad \left(\frac{V}{V}\right) \tag{1}$$

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance. Resistor arrays with 1% matching can be used with a tolerance greater than 1%.

Place the input resistors very close to the STH4010 to limit noise injection on the high-impedance nodes.

For optimal performance the gain should be set to 2 V/V or lower. Lower gain allows the STH4010 to operate at its best, and keeps a high voltage at the input making the inputs less susceptible to noise.

Decoupling Capacitor (C_S)

The STH4010 is a high-performance class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 µF, placed as close as possible to the device V_{DD} lead works best. Placing this decoupling capacitor close to the STH4010 is very important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 10 µF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

Input Capacitors (C_I)

The STH4010 does not require input coupling capacitors if the design uses a differential source that is biased from 0.5 V to V_{DD}– 0.8 V (shown in Figure 27). If the input signal is not biased within the recommended common-mode input range, if needing to use the input as a high pass filter (shown in Figure 28), or if using a single-ended source (shown in Figure 29), input coupling capacitors are required.

The input capacitors and input resistors form a high-pass filter with the corner frequency, f_c, determined in Equation 2.

$$f_C = \frac{1}{\left(2\pi R_I C_I\right)} \tag{2}$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application.

Equation 3 is reconfigured to solve for the input coupling capacitance.

$$C_I = \frac{1}{\left(2\pi R_I f_C\right)} \tag{3}$$

If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

For a flat low-frequency response, use large input coupling capacitors (1 µF). However, in a GSM phone the ground signal is fluctuating at 217 Hz, but the signal from the codec does not have the same 217 Hz fluctuation. The difference between the two signals is amplified, sent to the speaker, and heard as a 217 Hz hum.

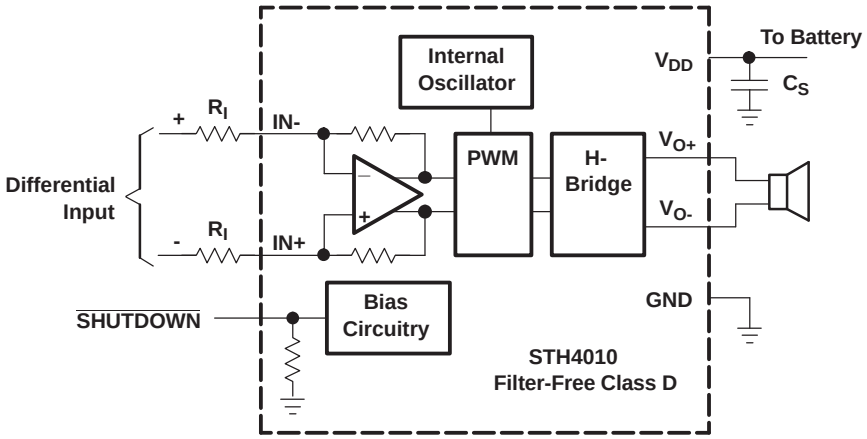


Figure 27. Typical STH4010 Application Schematic With Differential Input for a Wireless Phone

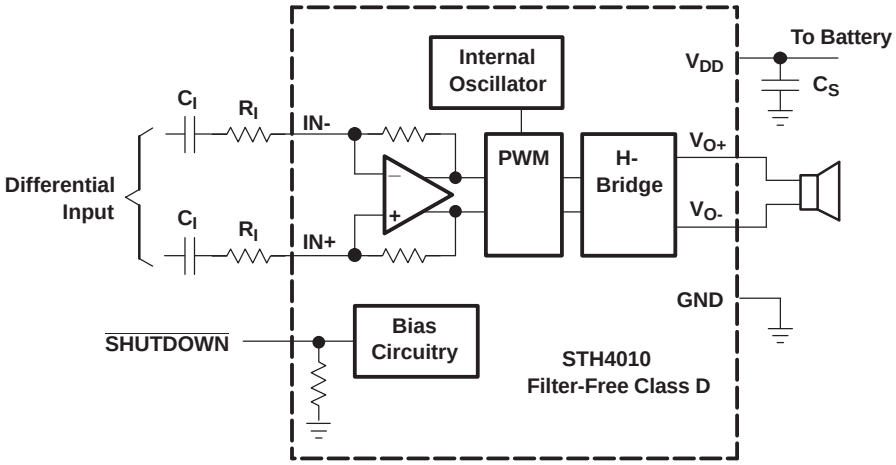


Figure 28. STH4010 Application Schematic With Differential Input and Input Capacitors

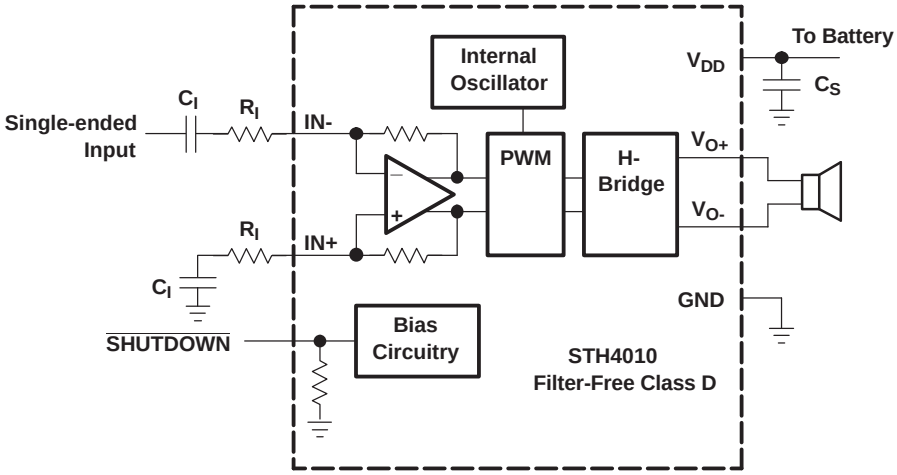


Figure 29. STH4010 Application Schematic With Single-Ended Input

SUMMING INPUT SIGNALS WITH THE STH4010

Most wireless phones or PDAs need to sum signals at the audio power amplifier or just have two signal sources that need separate gain. The STH4010 makes it easy to sum signals or use separate signal sources with different gains. Many phones now use the same speaker for the earpiece and ringer, where the wireless phone would require a much lower gain for the phone earpiece than for the ringer. PDAs and phones that have stereo headphones require summing of the right and left channels to output the stereo signal to the mono speaker.

Summing Two Differential Input Signals

Two extra resistors are needed for summing differential signals (a total of 5 components). The gain for each input source can be set independently (see Equation 4 and Equation 5, and Figure 30).

$$\text{Gain 1} = \frac{V_O}{V_{I1}} = \frac{2 \times 150\ k\Omega}{R_{I1}} \quad \left(\frac{V}{V}\right) \tag{4}$$

$$\text{Gain 2} = \frac{V_O}{V_{I2}} = \frac{2 \times 150\ k\Omega}{R_{I2}} \quad \left(\frac{V}{V}\right) \tag{5}$$

If summing left and right inputs with a gain of 1 V/V, use $R_{I1} = R_{I2} = 300\ k\Omega$.

If summing a ring tone and a phone signal, set the ring-tone gain to Gain 2 = 2 V/V, and the phone gain to gain 1 = 0.1 V/V. The resistor values would be. . .

R_{I1} = 3 MΩ, and = R_{I2} = 150 kΩ.

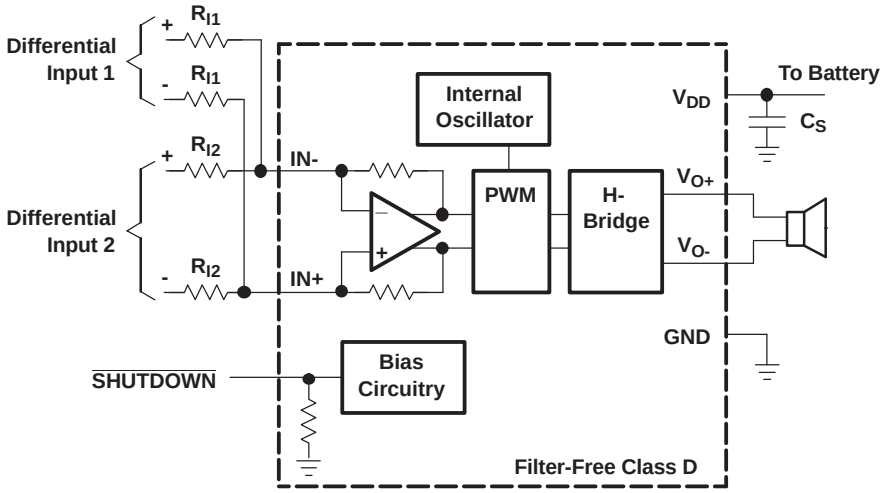


Figure 30. Application Schematic With STH4010 Summing Two Differential Inputs

Summing a Differential Input Signal and a Single-Ended Input Signal

Figure 31 shows how to sum a differential input signal and a single-ended input signal. Ground noise can couple in through IN+ with this method. It is better to use differential inputs. The corner frequency of the single-ended input is set by C_{I2}, shown in Equation 8. To assure that each input is balanced, the single-ended input must be driven by a low-impedance source even if the input is not in use

$$\text{Gain 1} = \frac{V_O}{V_{I1}} = \frac{2 \times 150\ k\Omega}{R_{I1}} \quad \left(\frac{V}{V}\right) \tag{6}$$

$$\text{Gain 2} = \frac{V_O}{V_{I2}} = \frac{2 \times 150\ k\Omega}{R_{I2}} \quad \left(\frac{V}{V}\right) \tag{7}$$

$$C_{I2} = \frac{1}{\left(2\pi\, R_{I2}\, f_{c2}\right)} \tag{8}$$

If summing a ring tone and a phone signal, the phone signal should use a differential input signal while the ring tone might be limited to a single-ended signal. Phone gain is set at gain 1 = 0.1 V/V, and the ring-tone gain is set to gain 2 = 2 V/V, the resistor values would be…

R_{I1} = 3 MΩ, and = R_{I2} = 150 kΩ.

The high pass corner frequency of the single-ended input is set by C_{I2}. If the desired corner frequency is less than 20 Hz...

$$C_{I2} > \frac{1}{(2\pi\ 150\,k\Omega\ 20\,Hz)} \quad (9)$$

$$C_{I2} > 53\,pF \quad (10)$$

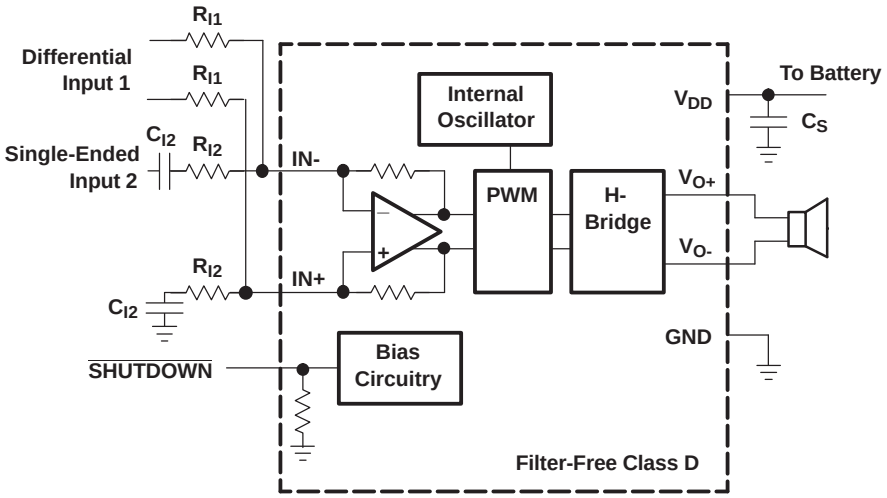


Figure 31. Application Schematic With STH4010 Summing Differential Input and Single-Ended Input Signals

Summing Two Single-Ended Input Signals

Four resistors and three capacitors are needed for summing single-ended input signals. The gain and corner frequencies (f_{c1} and f_{c2}) for each input source can be set independently (see Equation 11 through Equation 14, and Figure 32). Resistor, R_P, and capacitor, C_P, are needed on the IN+ terminal to match the impedance on the IN- terminal. The single-ended inputs must be driven by low impedance sources even if one of the inputs is not outputting an ac signal.

$$\text{Gain 1} = \frac{V_O}{V_{I1}} = \frac{2 \times 150\ k\Omega}{R_{I1}} \quad \left(\frac{V}{V}\right) \quad (11)$$

$$\text{Gain 2} = \frac{V_O}{V_{I2}} = \frac{2 \times 150\ k\Omega}{R_{I2}} \quad \left(\frac{V}{V}\right) \quad (12)$$

$$C_{I1} = \frac{1}{(2\pi\ R_{I1}\ f_{c1})} \quad (13)$$

$$C_{I2} = \frac{1}{(2\pi\ R_{I2}\ f_{c2})} \quad (14)$$

$$C_P = C_{I1} + C_{I2} \quad (15)$$

$$R_P = \frac{R_{I1} \times R_{I2}}{(R_{I1} + R_{I2})} \quad (16)$$

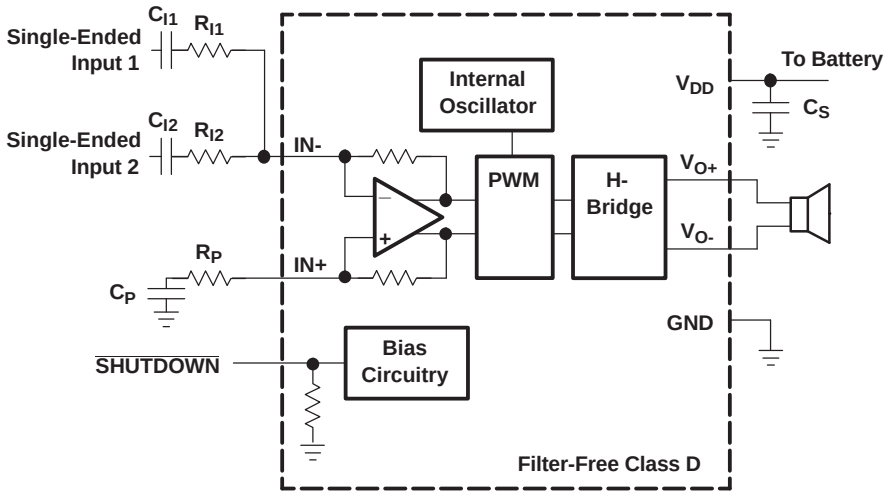


Figure 32. Application Schematic With STH4010 Summing Two Single-Ended Inputs

BOARD LAYOUT

In making the pad size for the WCSP balls, it is recommended that the layout use nonsolder mask defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. Figure 33 and Table 2 show the appropriate diameters for a WCSP layout. The STH4010 evaluation module (EVM) layout is shown in the next section as a layout example.

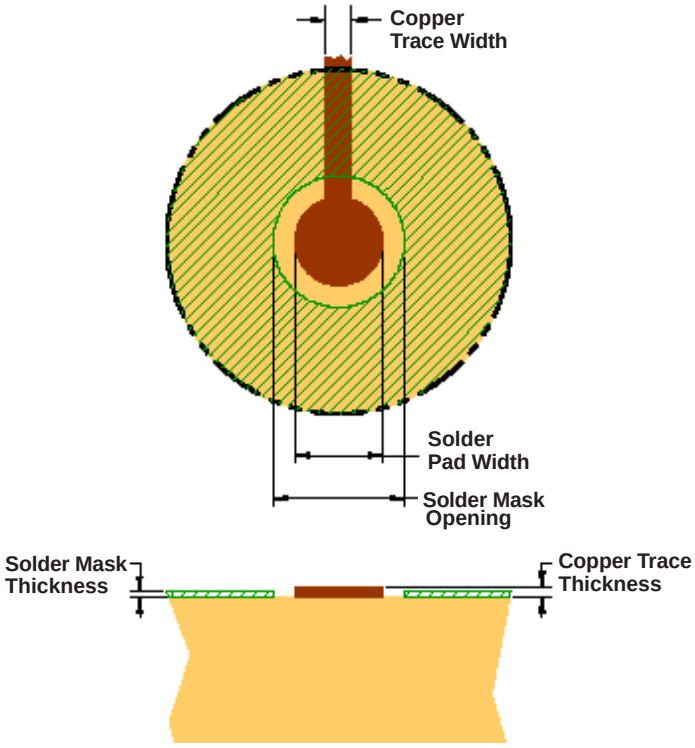


Figure 33. Land Pattern Dimensions

Table 2. Land Pattern Dimensions

SOLDER PAD DEFINITIONS	COPPER PAD	SOLDER MASK OPENING	COPPER THICKNESS	STENCIL OPENING	STENCIL THICKNESS
Nonsolder mask defined (NSMD)	275 µm (+0.0, –25 µm)	375 µm (+0.0, –25 µm)	1 oz max (32 µm)	275 µm x 275 µm Sq. (rounded corners)	125 µm thick

NOTES:

1. Circuit traces from NSMD defined PWB lands should be 75 µm to 100 µm wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand off and impact reliability.
2. Recommend solder paste is Type 3 or Type 4.
3. Best reilability results are achieved when the PWB laminate glass transition temperature is above the operating the range of the intended application.
4. For a PWB using a Ni/Au surface finish, the gold thickness should be less 0.5 µm to avoid a reduction in thermal fatigue performance.
5. Solder mask thickness should be less than 20 µm on top of the copper circuit pattern.
6. Best solder stencil preformance is achieved using laser cut stencils with electro polishing. Use of chemically etched stencils results in inferior solder paste volume control.
7. Trace routing away from WCSP device should be balanced in X and Y directions to avoid unintentional component movement due to solder wetting forces.

Component Location

Place all the external components very close to the STH4010. The input resistors need to be very close to the STH4010 input pins so noise does not couple on the high impedance nodes between the input resistors and the input amplifier of the STH4010. Placing the decoupling capacitor, CS, close to the STH4010 is important for the efficiency of the class-D amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

Trace Width

Recommended trace width at the solder balls is 75 µm to 100 µm to prevent solder wicking onto wider PCB traces. Figure 34 shows the layout of the STH4010 evaluation module (EVM).

For high current pins (V_{DD}, GND V_{O+}, and V_{O-}) of the STH4010, use 100-µm trace widths at the solder balls and at least 500-µm PCB traces to ensure proper performance and output power for the device.

For input pins (IN-, IN+, and $\overline{\text{SHUTDOWN}}$) of the STH4010, use 75-µm to 100-µm trace widths at the solder balls. IN- and IN+ pins need to run side-by-side to maximize common-mode noise cancellation. Placing input resistors, R_{IN}, as close to the STH4010 as possible is recommended.

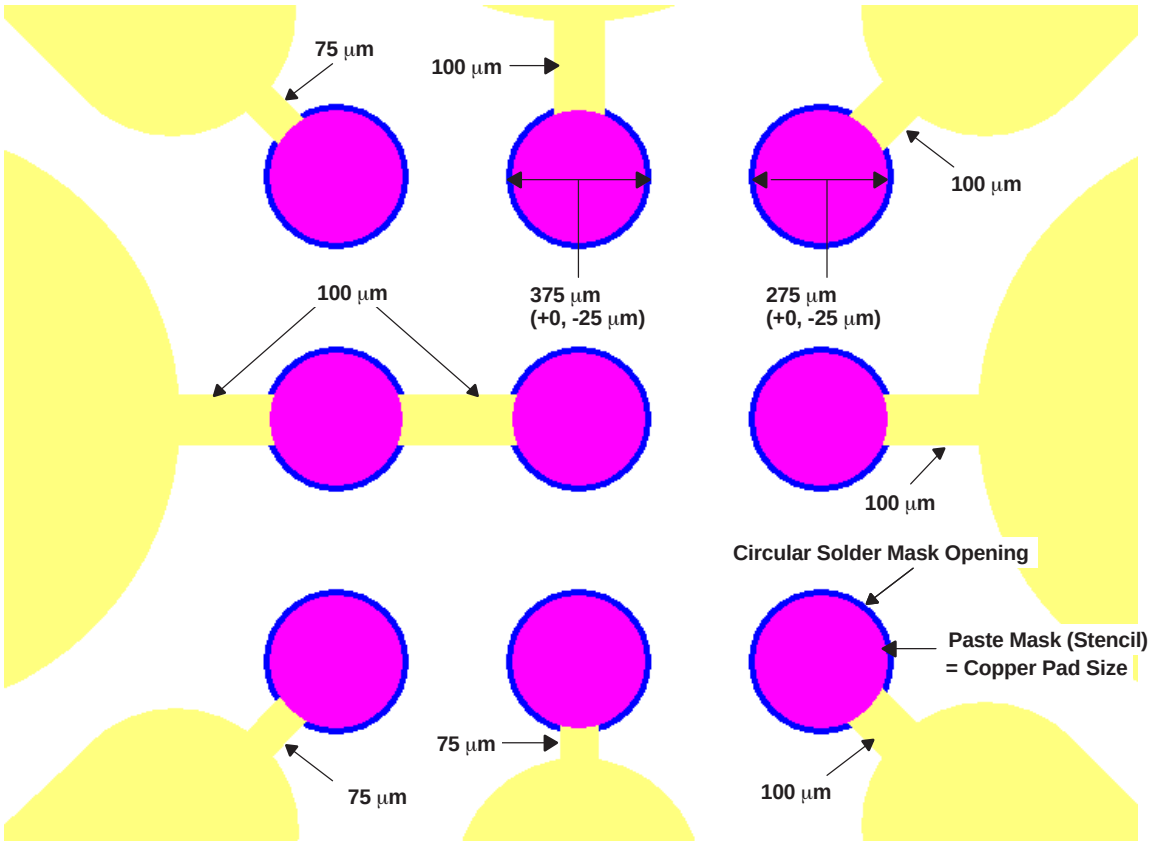


Figure 34. Close Up of STH4010 Land Pattern From STH4010 EVM

EFFICIENCY AND THERMAL INFORMATION

The maximum ambient temperature depends on the heat-sinking ability of the PCB system. The derating factor for the YEF and YEZ packages are shown in the dissipation rating table. Converting this to Θ_{JA}:

$$\theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.0078} = 128.2°C/W \quad (17)$$

Given Θ_{JA} of 128.2°C/W, the maximum allowable junction temperature of 125°C, and the maximum internal dissipation of 0.4 W (2.25 W, 4-Ω load, 5-V supply, from Figure 3), the maximum ambient temperature can be calculated with the following equation.

$$T_A Max = T_J Max - \theta_{JA} P_{Dmax} = 125 - 128.2\ (0.4) = 73.7°C \quad (18)$$

Equation 18 shows that the calculated maximum ambient temperature is 73.7°C at maximum power dissipation with a 5-V supply and 4-Ω a load, see Figure 3. The STH4010 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Also, using speakers more resistive than 4-Ω dramatically increases the thermal performance by reducing the output current and increasing the efficiency of the amplifier.

ELIMINATING THE OUTPUT FILTER WITH THE STH4010

This section focuses on why the user can eliminate the output filter with the STH4010

Effect on Audio

The class-D amplifier outputs a pulse-width modulated (PWM) square wave, which is the sum of the switching waveform and the amplified input audio signal. The human ear acts as a band-pass filter such that only the frequencies between approximately 20 Hz and 20 kHz are passed. The switching frequency components are much greater than 20 kHz, so the only signal heard is the amplified input audio signal.

Traditional Class-D Modulation Scheme

The traditional class-D modulation scheme, which is used in the STH4010 family, has a differential output where each output is 180 degrees out of phase and changes from ground to the supply voltage, V_{DD}. Therefore, the differential pre-filtered output varies between positive and negative V_{DD}, where filtered 50% duty cycle yields 0 volts across the load. The traditional class-D modulation scheme with voltage and current waveforms is shown in Figure 35. Note that even at an average of 0 volts across the load (50% duty cycle), the current to the load is high causing a high loss and thus causing a high supply current.

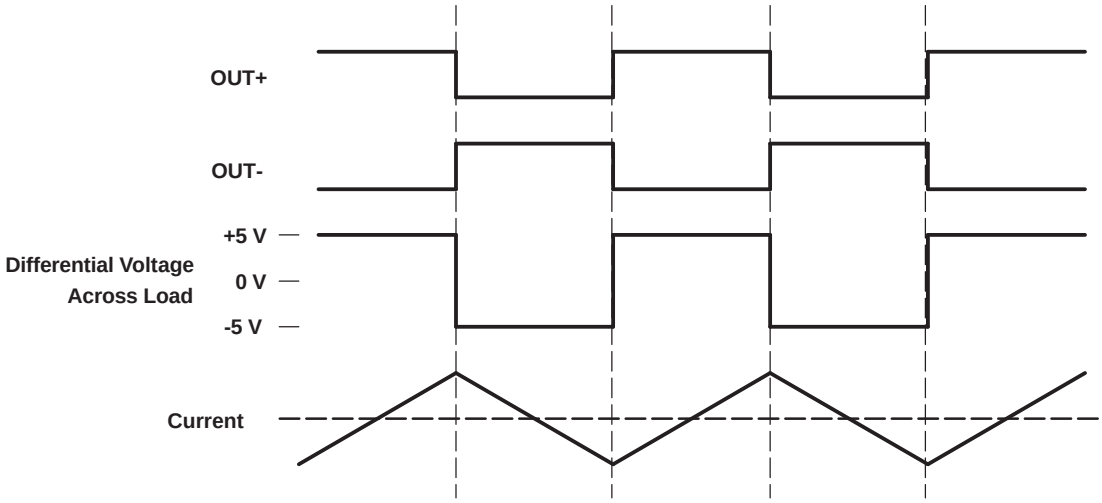


Figure 35. Traditional Class-D Modulation Scheme's Output Voltage and Current Waveforms Into an Inductive Load With no Input

STH4010 Modulation Scheme

The STH4010 uses a modulation scheme that still has each output switching from 0 to the supply voltage. However, OUT+ and OUT- are now in phase with each other with no input. The duty cycle of OUT+ is greater than 50% and OUT- is less than 50% for positive voltages. The duty cycle of OUT+ is less than 50% and OUT- is greater than 50% for negative voltages. The voltage across the load sits at 0 volts throughout most of the switching period greatly reducing the switching current, which reduces any I^2R losses in the load.

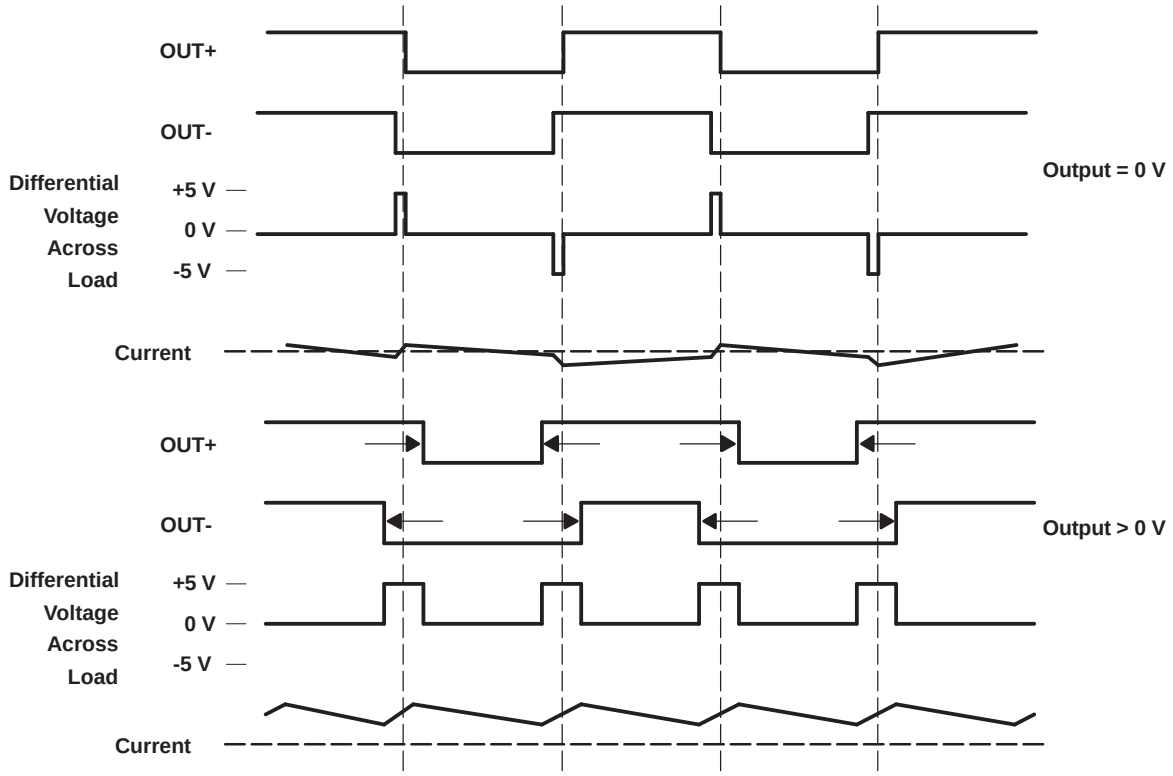


Figure 36. The STH4010 Output Voltage and Current Waveforms Into an Inductive Load

Efficiency: Why You Must Use a Filter With the Traditional Class-D Modulation Scheme

The main reason that the traditional class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is $2 \times V_{DD}$ and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The STH4010 modulation scheme has very little loss in the load without a filter because the pulses are very short and the change in voltage is V_{DD} instead of $2 \times V_{DD}$. As the output power increases, the pulses widen making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance than the speaker that results in less power dissipated, which increases efficiency.

Effects of Applying a Square Wave Into a Speaker

If the amplitude of a square wave is high enough and the frequency of the square wave is within the bandwidth of the speaker, a square wave could cause the voice coil to jump out of the air gap and/or scar the voice coil. A 250-kHz switching frequency, however, is not significant because the speaker cone movement is proportional to $1/f^2$ for frequencies beyond the audio band. Therefore, the amount of cone movement at the switching frequency is very small. However, damage could occur to the speaker if the voice coil is not designed to handle the additional power. To size the speaker for added power, the ripple current dissipated in the load needs to be calculated by subtracting the theoretical supplied power, $P_{SUP\ THEORETICAL}$, from the actual supply power, P_{SUP}, at maximum output power, P_{OUT}. The switching power dissipated in the speaker is the inverse of the measured efficiency, $\eta_{MEASURED}$, minus the theoretical efficiency, $\eta_{THEORETICAL}$.

$$P_{SPKR} = P_{SUP} - P_{SUP\ THEORETICAL} \text{ (at max output power)} \quad (19)$$

$$P_{SPKR} = \frac{P_{SUP}}{P_{OUT}} - \frac{P_{SUP\ THEORETICAL}}{P_{OUT}} \text{ (at max output power)} \quad (20)$$

$$P_{SPKR} = P_{OUT}\left(\frac{1}{\eta_{MEASURED}} - \frac{1}{\eta_{THEORETICAL}}\right) \text{ (at max output power)} \quad (21)$$

$$\eta THEORETICAL = \frac{R_L}{R_L + 2r_{DS(on)}} \text{ (at max output power)} \quad (22)$$

The maximum efficiency of the STH4010 with a 3.6 V supply and an 8-Ω load is 86% from Equation 22. Using equation Equation 21 with the efficiency at maximum power (84%), we see that there is an additional 17 mW dissipated in the speaker. The added power dissipated in the speaker is not an issue as long as it is taken into account when choosing the speaker.

When to Use an Output Filter

Design the STH4010 without an output filter if the traces from amplifier to speaker are short. The STH4010 passed FCC and CE radiated emissions with no shielding with speaker trace wires 100 mm long or less. Wireless handsets and PDAs are great applications for class-D without a filter.

A ferrite bead filter can often be used if the design is failing radiated emissions without an LC filter, and the frequency sensitive circuit is greater than 1 MHz. This is good for circuits that just have to pass FCC and CE because FCC and CE only test radiated emissions greater than 30 MHz. If choosing a ferrite bead, choose one with high impedance at high frequencies, but very low impedance at low frequencies.

Use an LC output filter if there are low frequency (< 1 MHz) EMI sensitive circuits and/or there are long leads from amplifier to speaker.

Figure 37 and Figure 38 show typical ferrite bead and LC output filters.

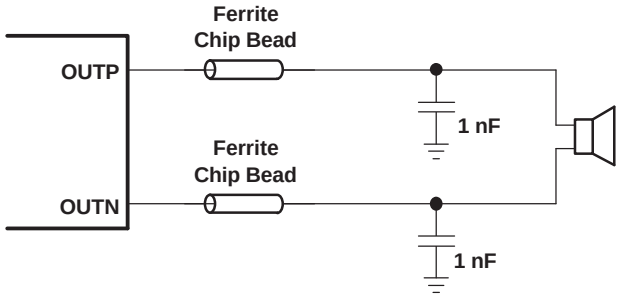


Figure 37. Typical Ferrite Chip Bead Filter (Chip bead example: NEC/Tokin: N2012ZPS121)

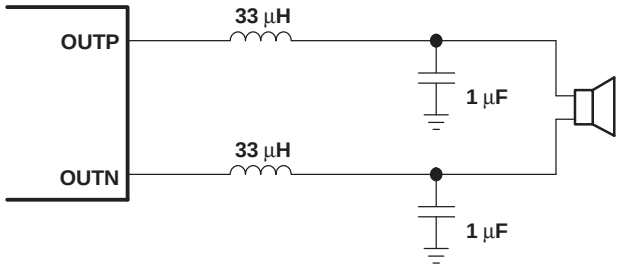


Figure 38. Typical LC Output Filter, Cutoff Frequency of 27 kHz

PACKAGING INFORMATION

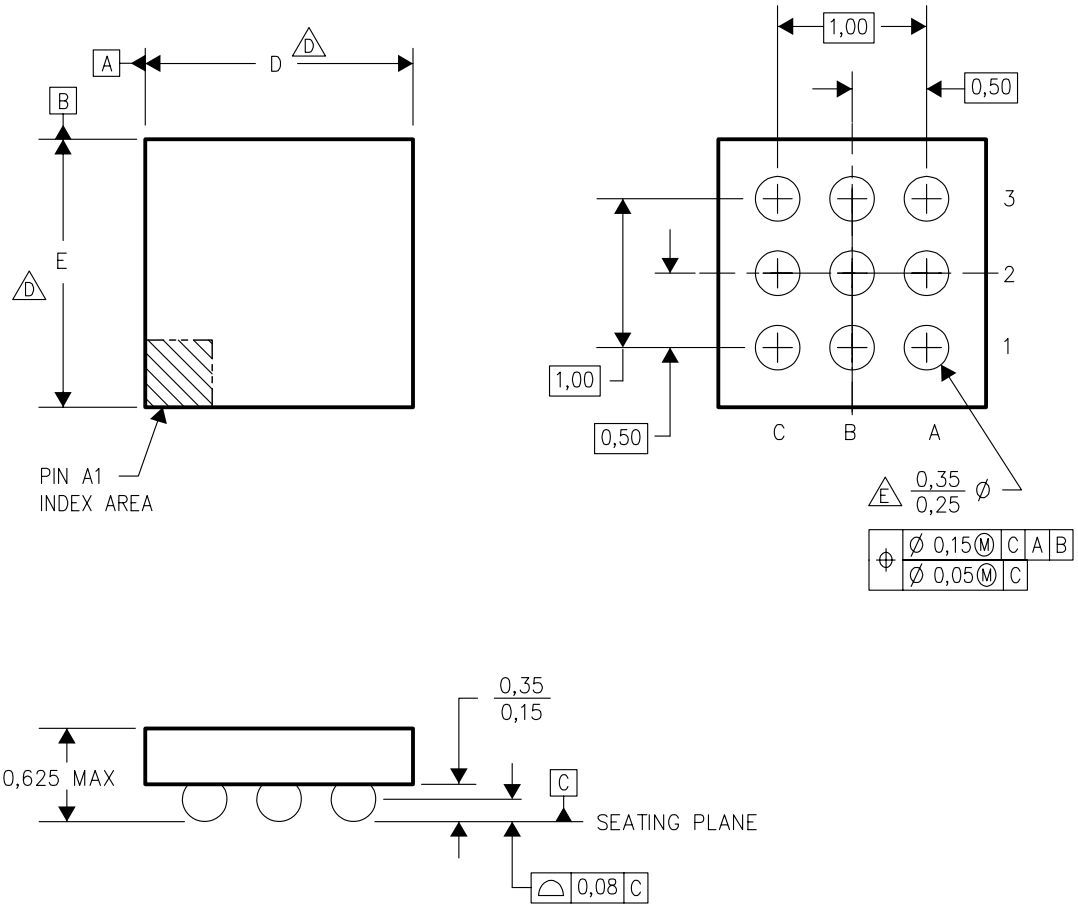
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
STH4010YEFR	ACTIVE	XCEPT	YEF	9	3000	TBD	Call TI	Level-1-240C-UNLIM
STH4010YEFT	ACTIVE	XCEPT	YEF	9	250	TBD	SNPB	Level-1-240C-UNLIM
STH4010YZFR	ACTIVE	DSBGA	YZF	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
STH4010YZFT	ACTIVE	DSBGA	YZF	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.sth-semico.comt for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

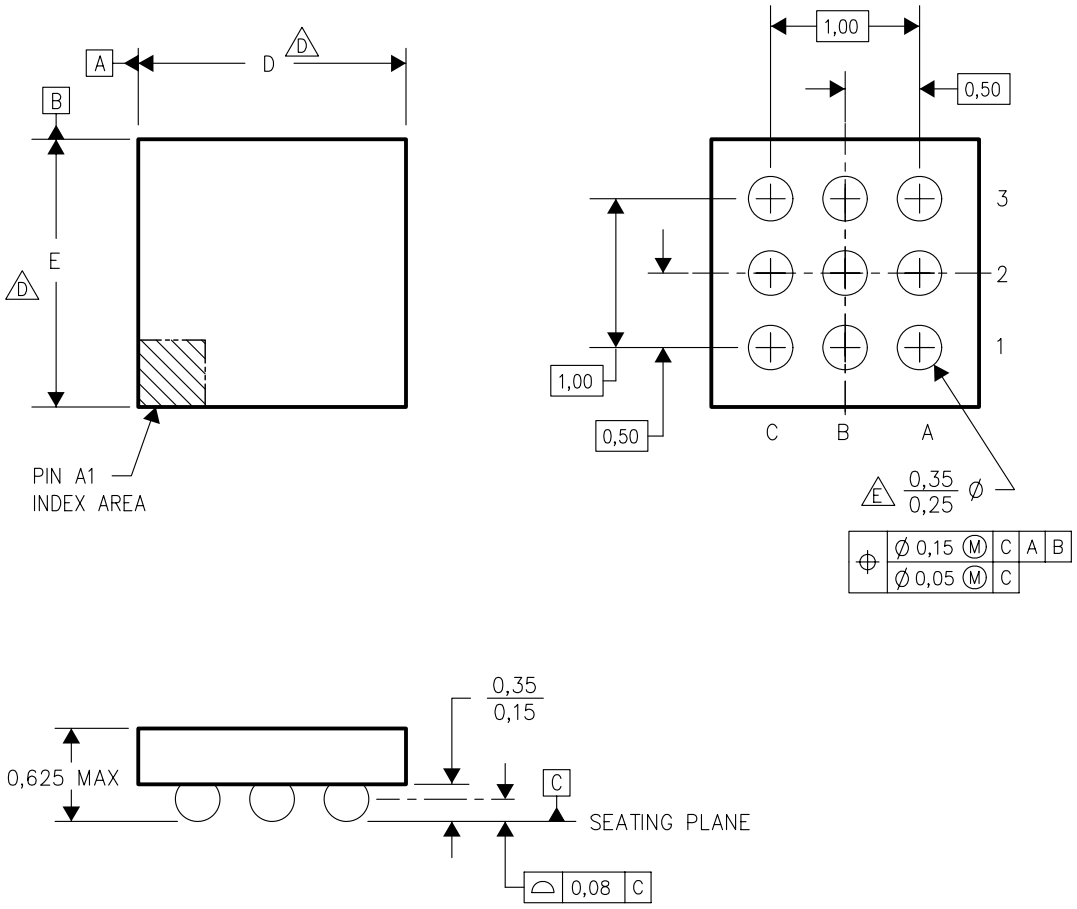
YEF (S–XBGA–N9) DIE–SIZE BALL GRID ARRAY



4204181/E 04/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.
D. Devices in YEF package can have dimension D ranging from 1.35 to 2.15 mm and dimension E ranging from 1.35 to 2.15 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E. Reference Product Data Sheet for array population. 3 x 3 matrix pattern is shown for illustration only.
F. This package contains tin–lead (SnPb) balls. Refer to YZF (Drawing #4205058) for lead–free balls.

YZF (S–XBGA–N9) DIE–SIZE BALL GRID ARRAY



4205058–3/E 11/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Devices in YZF package can have dimension D ranging from 1.35 to 2.15 mm and dimension E ranging from 1.35 to 2.15 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E Reference Product Data Sheet for array population. 3 x 3 matrix pattern is shown for illustration only.
F. This package contains lead–free balls. Refer to YEF (Drawing #4204181) for tin–lead (SnPb) balls.